ANALOG DEVICES

# Precision, 16 MHz CBFET Op Amp

# AD845

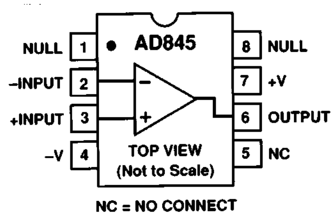
## FEATURES
**Replaces Hybrid Amplifiers in Many Applications**

**AC PERFORMANCE:**
**Settles to 0.01% in 350 ns**
**100 V/μs Slew Rate**
**12.8 MHz min Unity-Gain Bandwidth**
**1.75 MHz Full-Power Bandwidth at 20 V p-p**

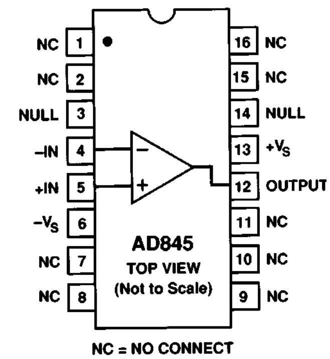
**DC PERFORMANCE:**
**0.25 mV max Input Offset Voltage**
**5 μV/°C max Offset Voltage Drift**
**0.5 nA Input Bias Current**
**250 V/mV min Open-Loop Gain**
**4 μV p-p max Voltage Noise, 0.1 Hz to 10 Hz**
**94 dB min CMRR**
**Available in Plastic Mini-DIP, Hermetic Cerdip and SOIC Packages. Also Available in Tape and Reel in Accordance with EIA-481A Standard**

## CONNECTION DIAGRAMS

**Plastic Mini-DIP (N) Package and Cerdip (Q) Package**




**16-Pin SOIC (R-16) Package**




## PRODUCT DESCRIPTION

The AD845 is a fast, precise, N channel JFET input, monolithic operational amplifier. It is fabricated using Analog Devices' complementary bipolar (CB) process. Advanced laser-wafer trimming technology enables the very low input offset voltage and offset voltage drift performance to be realized. This precision, when coupled with a slew rate of 100 V/μs, a stable unity-gain bandwidth of 16 MHz, and a settling time of 350 ns 0.01%—while driving a parallel load of 100 pF and 500 Ω—represents a combination of features unmatched by any FET input IC amplifier. The AD845 can easily be used to upgrade many existing designs which use BiFET or FET input hybrid amplifiers and, in some cases, those which use bipolar input op amps.

The AD845 is ideal for use in applications such as active filters, high speed integrators, photo diode preamps, sample-and-hold amplifiers, log amplifiers, and in buffering A/D and D/A converters. The 250 μV max input offset voltage makes offset nulling unnecessary in many applications. The common-mode rejection ratio of 110 dB over a ±10 V input voltage range represents exceptional performance for a JFET input high speed op amp. This, together with a minimum open-loop gain of 250 V/mV ensures that 12-bit performance is achieved, even in unity-gain buffer circuits.

The AD845 conforms to the standard op amp pinout except that offset nulling is to V+. The AD845J and AD845K grade devices are available specified to operate over the commercial 0°C to +70°C temperature range. AD845A and AD845B devices are specified for operation over the –40°C to +85°C industrial temperature range. The AD845S is specified to operate over the full military temperature range of –55°C to +125°C. Both the industrial and military versions are available in 8-pin cerdip packages. The commercial version is available in an 8-pin plastic mini-DIP and 16-pin SOIC; "J" and "S" grade chips are also available.

## PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time, and dc precision of the AD845 make it ideal for high speed applications requiring 12-bit accuracy.
2. The performance of circuits using the LF400, HA2520/2/5, HA2620/2/5, 3550, OPA605, and LH0062 can be upgraded in most cases.
3. The AD845 is unity-gain stable and internally compensated.
4. The AD845 is specified while driving 100 pF/500 Ω loads.

REV. D



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Tel: 617/329-4700 Fax: 617/326-8703

# AD845–SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

| Model | Conditions | AD845J/A Min | AD845J/A Typ | AD845J/A Max | AD845K/B Min | AD845K/B Typ | AD845K/B Max | AD845S Min | AD845S Typ | AD845S Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| INPUT OFFSET VOLTAGE[1] | | | | | | | | | | | |
| Initial Offset | | | 0.7 | **1.5** | | 0.1 | **0.25** | | 0.25 | **1.0** | mV |
| | $T_{MIN}$–$T_{MAX}$ | | | 2.5 | | | **0.4** | | | 2.0 | mV |
| Offset Drift | | | | 20 | | 1.5 | **5.0** | | | **10** | µV/°C |
| INPUT BIAS CURRENT[2] | | | | | | | | | | | |
| Initial | $V_{CM}$ = 0 V | | 0.75 | **2** | | 0.5 | **1** | | 0.75 | **2** | nA |
| | $T_{MIN}$–$T_{MAX}$ | | | 45/75 | | | **18/38** | | | **500** | nA |
| INPUT OFFSET CURRENT | | | | | | | | | | | |
| Initial | $V_{CM}$ = 0 V | | 25 | **300** | | 15 | **100** | | 25 | **300** | pA |
| | $T_{MIN}$–$T_{MAX}$ | | | 3/6.5 | | | **1.2/2.6** | | | **20** | nA |
| INPUT CHARACTERISTICS | | | | | | | | | | | |
| Input Resistance | | | $10^{11}$ | | | $10^{11}$ | | | $10^{11}$ | | kΩ |
| Input Capacitance | | | 4.0 | | | 4.0 | | | 4.0 | | pF |
| INPUT VOLTAGE RANGE | | | | | | | | | | | |
| Differential | | | ±20 | | | ±20 | | | ±20 | | V |
| Common Mode | | **±10** | +10.5/–13 | | **±10** | +10.5/–13 | | **±10** | +10.5/–13 | | V |
| Common-Mode Rejection | $V_{CM}$ = ±10 V | **86** | 110 | | **94** | 113 | | **86** | 110 | | dB |
| INPUT VOLTAGE NOISE | 0.1 Hz to 10 Hz | | 4 | | | 4 | | | 4 | | µV p-p |
| | f = 10 Hz | | 80 | | | 80 | | | 80 | | nV/√Hz |
| | f = 100 Hz | | 60 | | | 60 | | | 60 | | nV/√Hz |
| | f = 1 kHz | | 25 | | | 25 | | | 25 | | nV/√Hz |
| | f = 10 kHz | | 18 | | | 18 | | | 18 | | nV/√Hz |
| | f = 100 kHz | | 12 | | | 12 | | | 12 | | nV/√Hz |
| INPUT CURRENT NOISE | f = 1 kHz | | 0.1 | | | 0.1 | | | 0.1 | | pA/√Hz |
| OPEN-LOOP GAIN | $V_O$ = ±10 V | | | | | | | | | | |
| | $R_{LOAD}$ ≥ 2 kΩ | **200** | 500 | | **250** | 500 | | **200** | 500 | | V/mV |
| | $R_{LOAD}$ ≥ 500 Ω | **100** | 250 | | **125** | 250 | | **100** | 250 | | V/mV |
| | $T_{MIN}$–$T_{MAX}$ | 70 | | | **75** | | | **50** | | | V/mV |
| OUTPUT CHARACTERISTICS | | | | | | | | | | | |
| Voltage | $R_{LOAD}$ ≥ 500 Ω | **±12.5** | | | **±12.5** | | | **±12.5** | | | V |
| Current | Short Circuit | | 50 | | | 50 | | | 50 | | mA |
| Output Resistance | Open Loop | | 5 | | | 5 | | | 5 | | Ω |
| FREQUENCY RESPONSE | | | | | | | | | | | |
| Small Signal | Unity Gain | 12.8 | 16 | | 13.6 | 16 | | 13.6 | 16 | | MHz |
| Full Power Bandwidth[3] | $V_O$ = ±10 V | | | | | | | | | | |
| | $R_{LOAD}$ = 500 Ω | | 1.75 | | | 1.75 | | | 1.75 | | MHz |
| Rise Time | | | 20 | | | 20 | | | 20 | | ns |
| Overshoot | | | 20 | | | 20 | | | 20 | | % |
| Slew Rate | | **80** | 100 | | **94** | 100 | | **94** | 100 | | V/µs |
| Settling Time | 10 V Step | | | | | | | | | | |
| | $C_{LOAD}$ = 100 pF | | | | | | | | | | |
| | $R_{LOAD}$ = 500 Ω | | | | | | | | | | |
| | to 0.01% | | 350 | | | 350 | 500 | | 350 | 500 | ns |
| | to 0.1% | | 250 | | | 250 | | | 250 | | ns |
| DIFFERENTIAL GAIN | f = 4.4 MHz | | 0.04 | | | 0.04 | | | 0.04 | | % |
| DIFFERENTIAL PHASE | f = 4.4 MHz | | 0.02 | | | 0.02 | | | 0.02 | | Degree |
| POWER SUPPLY | | | | | | | | | | | |
| Rated Performance | | | ±15 | | | ±15 | | | ±15 | | V |
| Operating Range | | **±4.75** | | **±18** | **±4.75** | | **±18** | **±4.75** | | **±18** | V |
| Rejection Ratio | $V_S$ = ±5 to ±15 V | **88** | 110 | | **95** | 113 | | **88** | 110 | | dB |
| Quiescent Current | $T_{MIN}$ to $T_{MAX}$ | | 10 | 12 | | 10 | **12** | | 10 | **12** | mA |

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at $T_A$ = +25°C.

[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A$ = +25°C.

[3]FPBW = slew rate/2 π V peak.

[4]"S" grade $T_{MIN}$–$T_{MAX}$ are tested with automatic test equipment at $T_A$ = –55°C and $T_A$ = +125°C.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

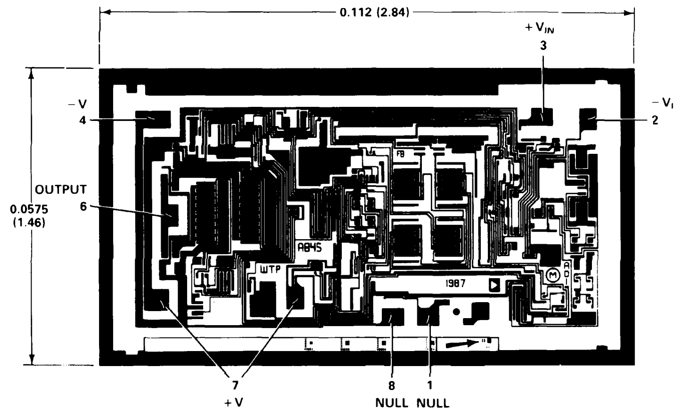
## ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±18 V
Internal Power Dissipation[2]
Plastic Mini-DIP . . . . . . . . . . . . . . . . . . . . . . . . . 1.6 Watts
Cerdip . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1.4 Watts
16-Pin SOIC . . . . . . . . . . . . . . . . . . . . . . . . . . . 1.5 Watts
Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $+V_S$
Output Short-Circuit Duration . . . . . . . . . . . . . . . . Indefinite
Differential Input Voltage . . . . . . . . . . . . . . . . . . $+V_S$ and $-V_S$
Storage Temperature Range
Q . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –65°C to +150°C
N, R . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability .
[2]Mini-DIP package: $\theta_{JA}$ = 100°C/watt; cerdip package: $\theta_{JA}$ = 110°C/watt. SOIC package: $\theta_{JA}$ = 100°C/W.

## METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.




SUBSTRATE CONNECTED TO $+V_S$

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option* |
|---|---|---|---|
| AD845JN | 0°C to +70°C | 8-Pin Plastic Mini-DIP | N-8 |
| AD845KN | 0°C to +70°C | 8-Pin Plastic Mini-DIP | N-8 |
| AD845JR-16 | 0°C to +70°C | 16-Pin SOIC | R-16 |
| AD845AQ | –40°C to +85°C | 8-Pin Cerdip | Q-8 |
| AD845BQ | –40°C to +85°C | 8-Pin Cerdip | Q-8 |
| AD845SQ | –55°C to +125°C | 8-Pin Cerdip | Q-8 |
| AD845SQ/883B | –55°C to +125°C | 8-Pin Cerdip | Q-8 |
| 5962-8964501PA | –55°C to +125°C | 8-Pin Cerdip | Q-8 |
| AD845JCHIPS | 0°C to +70°C | Die | |
| AD845SCHIPS | –55°C to +125°C | Die | |
| AD845JR-16-REEL | 0°C to +70°C | Tape & Reel | |
| AD845JR-16-REEL7 | 0°C to +70°C | Tape & Reel | |

*N = Plastic DIP: Q = Cerdip; R = Small Outline IC (SOIC).

*Common-Mode Voltage*

*Limit vs. Temperature*

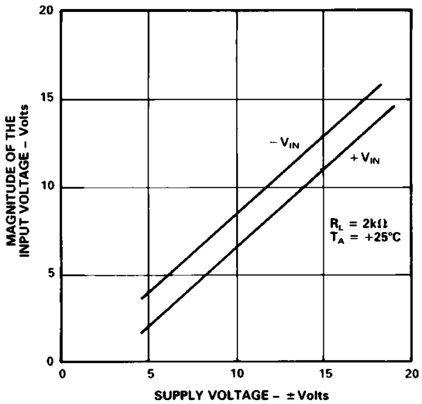



*Figure 1. Input Voltage Swing vs. Supply Voltage*

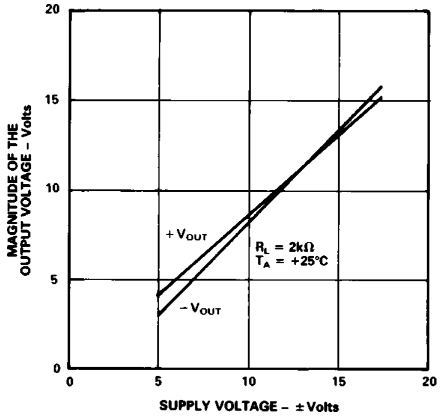



*Figure 2. Output Voltage Swing vs. Supply Voltage*

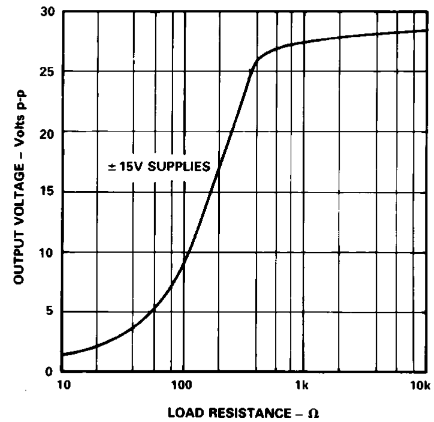



*Figure 3. Output Voltage Swing vs. Resistive Load*

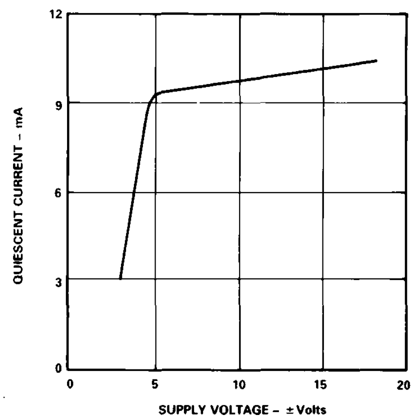



*Figure 4. Quiescent Current vs. Supply Voltage*

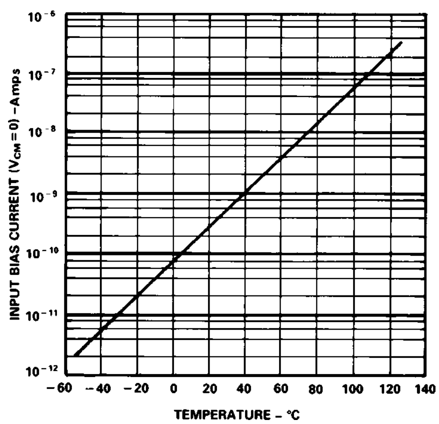



*Figure 5. Input Bias Current vs. Temperature*

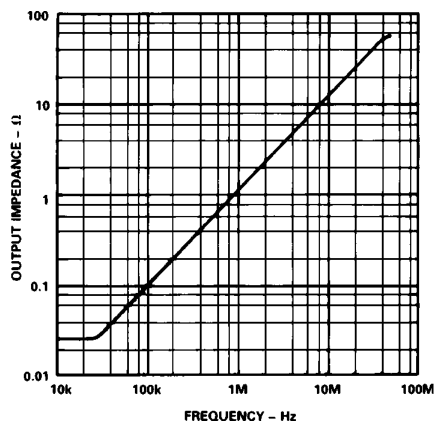



*Figure 6. Magnitude of Output Impedance vs. Frequency*

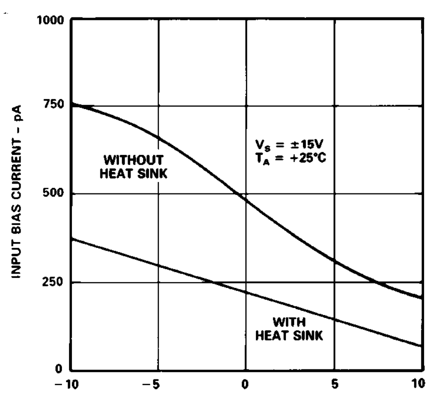



*Figure 7. Input Bias Current vs.*

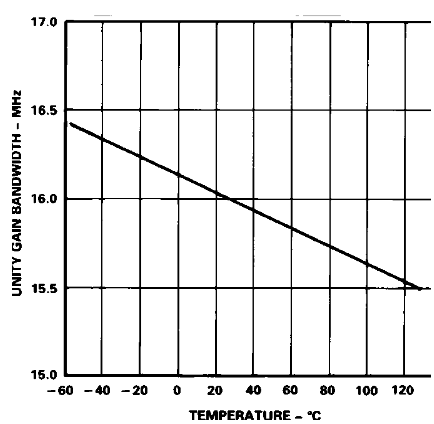



*Figure 8. Short-Circuit Current*

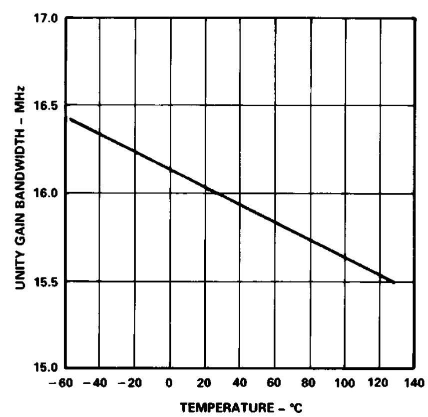



*Figure 9. Unity-Gain Bandwidth*

*vs. Temperature*

*vs. Frequency*

*Spectral Density*

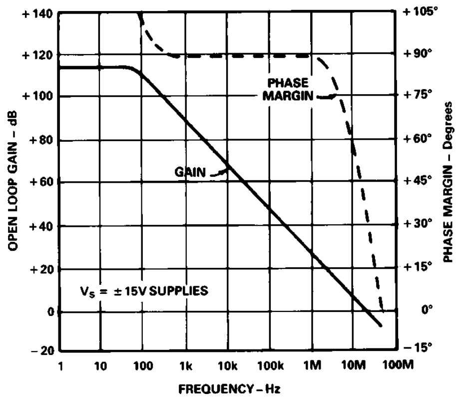



*Figure 10. Open-Loop Gain and Phase Margin vs. Frequency*

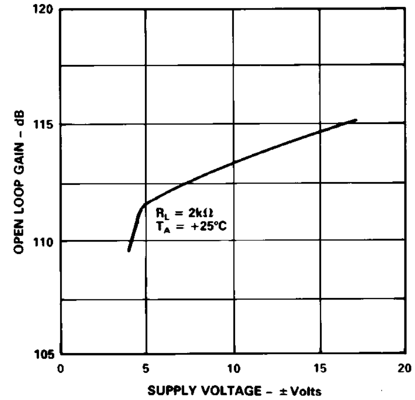



*Figure 11. Open-Loop Gain vs. Supply Voltage*

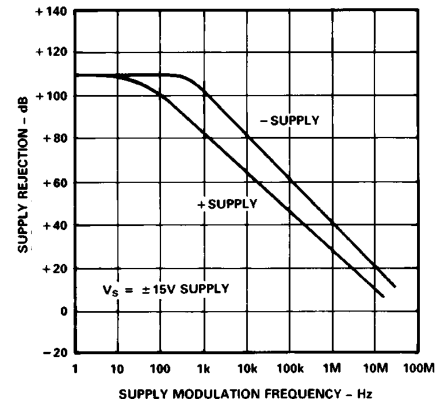



*Figure 12. Power Supply Rejection vs. Frequency*

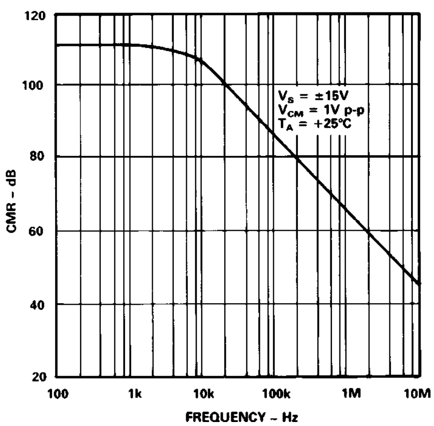



*Figure 13. Common-Mode Rejection vs. Frequency*

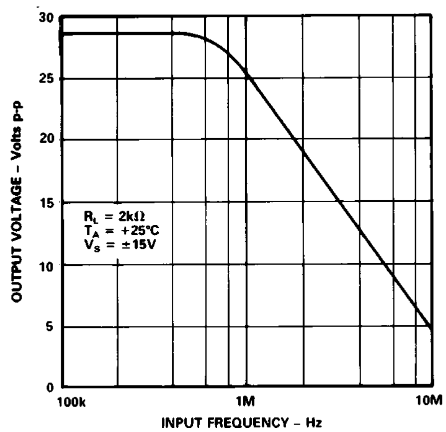



*Figure 14. Large Signal Frequency Response*

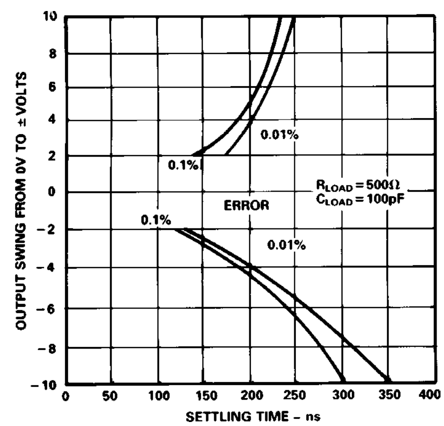



*Figure 15. Output Swing and Error vs. Settling Time*

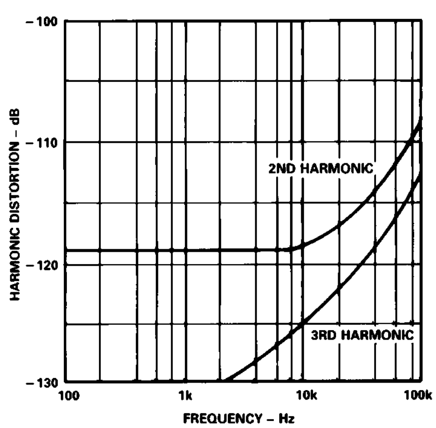



*Figure 16. Harmonic Distortion*

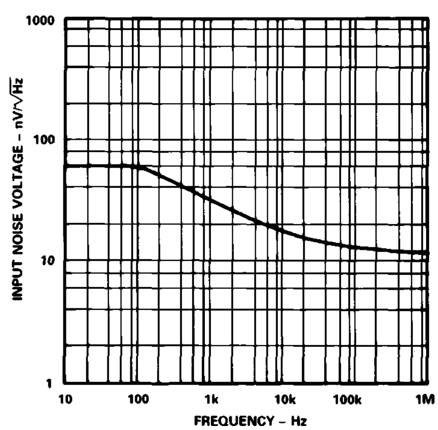



*Figure 17. Input Noise Voltage*

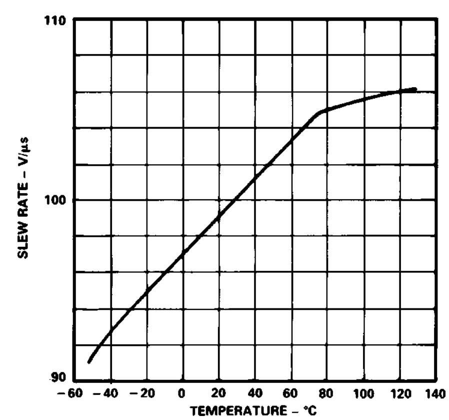



*Figure 18. Slew Rate vs. Temperature*

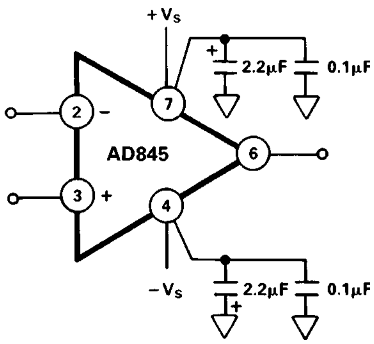



Figure 19. Recommended Power Supply Bypassing

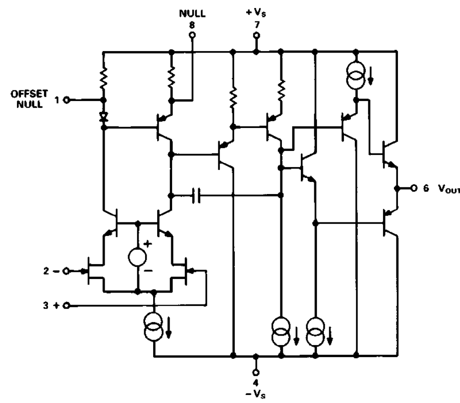



Figure 20. AD845 Simplified Schematic

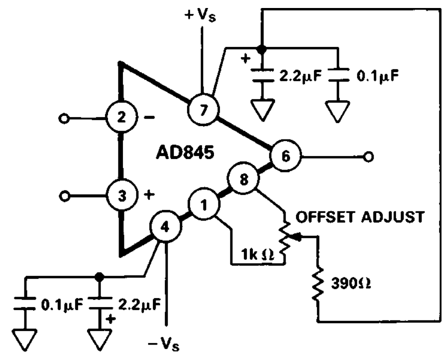



Figure 21. Offset Null Configuration

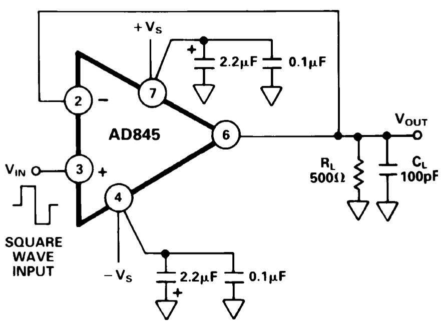



Figure 22a. Unity-Gain Follower

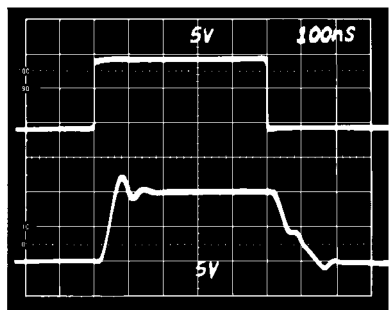



Figure 22b. Unity-Gain Follower Large Signal Pulse Response

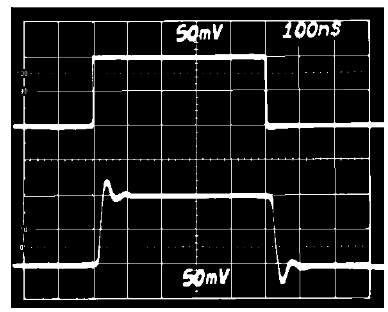



Figure 22c. Unity-Gain Follower Small Signal Pulse Response

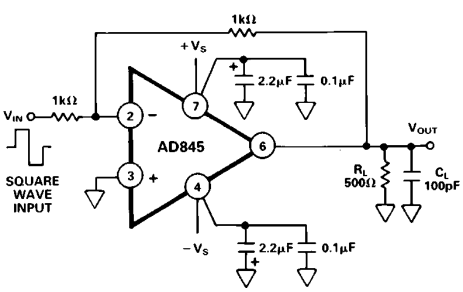



Figure 23a. Unity-Gain Inverter

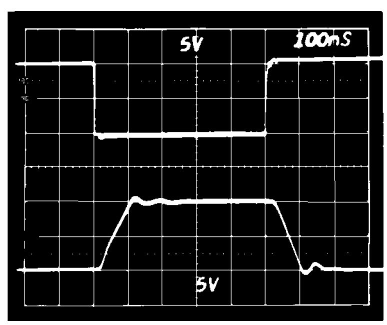



Figure 23b. Unity-Gain Inverter Large Signal Pulse Response

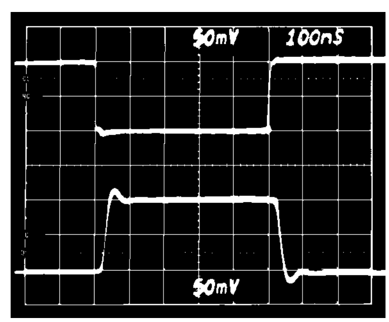



Figure 23c. Unity-Gain Inverter Small Signal Pulse Response

## MEASURING AD845 SETTLING TIME

The Figure 24 shows the AD845 settling time performance. This measurement was accomplished by driving the amplifier in the unity-gain inverting mode with a fast pulse generator. The input summing junction was measured using false nulling techniques.

Settling time is defined as:

The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

Components of settling time include:

1. Propagation time through the amplifier
2. Slewing time to approach the final output value
3. Recovery time from overload associated with the slewing
4. Linear settling to within a specified error band.

These individual components can easily be seen in Figure 24. Settling time is extremely important in high speed applications where the current output of a DAC must be converted to a voltage. When driving a 500 Ω load in parallel with a 100 pF capacitor, the AD845 settles to 0.1% in 250 ns and to 0.01% in 310 ns.

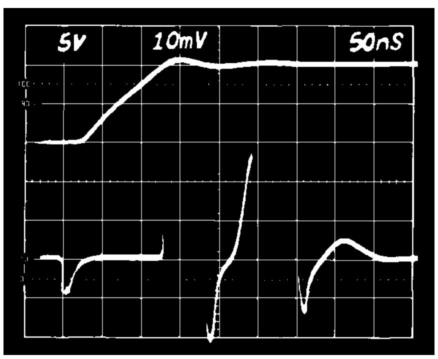



*Figure 24. Settling Characteristics 0 V to 10 V Step Upper Trace: Output of AD845 Under Test (5 V/Div) Lower Trace: Error Voltage (1 mV/Div)*

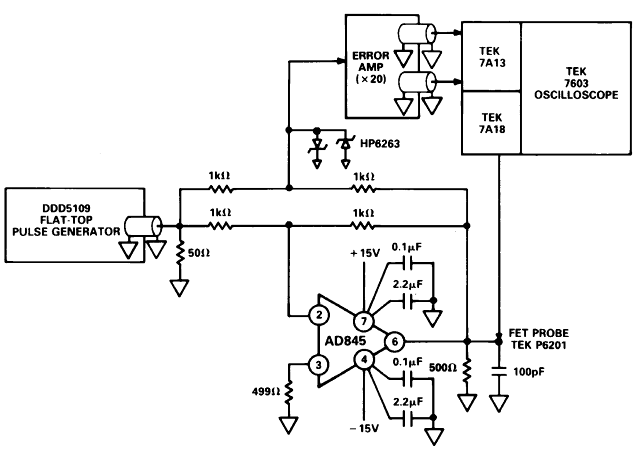



*Figure 25. Settling Time Test Circuit*

## A HIGH SPEED INSTRUMENTATION AMP

The three op amp instrumentation amplifier circuit shown in Figure 26 can provide a range of gains from unity up to 1000 and higher. The instrumentation amplifier configuration features high common-mode rejection, balanced differential inputs and stable, accurately defined gain. Low input bias currents and fast settling are achieved with the FET input AD845.

Most monolithic instrumentation amplifiers do not have the high frequency performance of the circuit in Figure 26. The circuit bandwidth is 10.9 MHz at a gain of 1 and 8.8 MHz at a gain of 10; settling time for the entire circuit is 900 ns to 0.01% for a 10 V step (Gain = 10).

The capacitors employed in this circuit greatly improve the amplifier's settling time and phase margin.

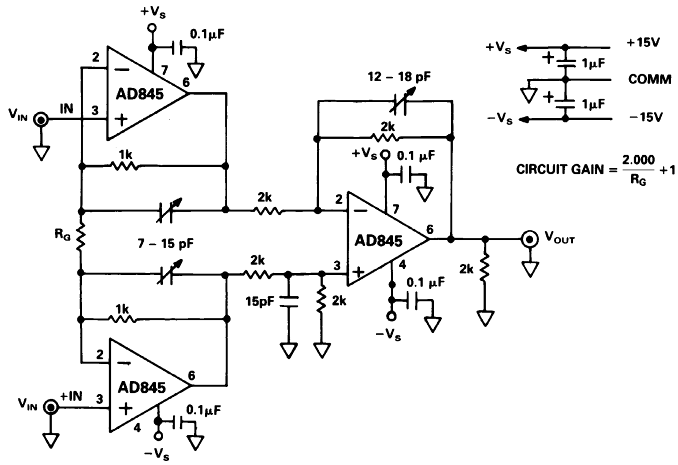



*Figure 26. High Performance, High Speed Instrumentation Amplifier*

**Table I. Performance Summary for the Three Op Amp Instrumentation Amplifier Circuit**

| 3 Op-Amp In-Amp | | | |
|---|---|---|---|
| **Gain** | **$R_G$** | **Small Signal Bandwidth** | **Settling Time to 0.01%** |
| 1 | Open | 10.9 MHz | 500 ns |
| 2 | 2k | 8.8 MHz | 500 ns |
| 10 | 226 Ω | 2.6 MHz | 900 ns |
| 100 | 20 Ω | 290 kHz | 7.5 µs |

Note: Resistors around the amplifiers' input pins need to be small enough in value so that the RC time constant they form, with stray circuit capacitance, does not reduce circuit bandwidth.

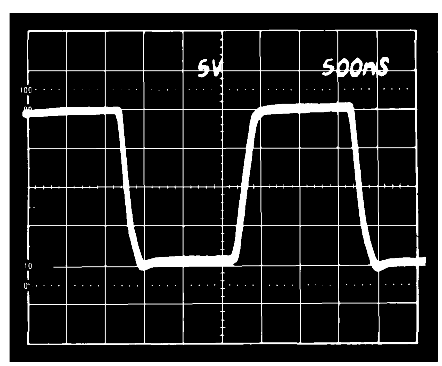



*Figure 27. The Pulse Response of the Three Op Amp Instrumentation Amplifier. Gain = 1, Horizontal Scale: 0.5 ms/Div; Vertical Scale: 5 V/Div*

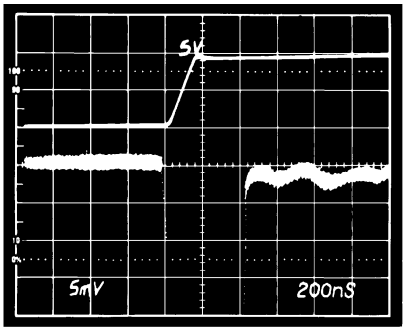



*Figure 28a. Settling Time of the Three Op Amp Instrumentation Amplifier. Horizontal Scale: 200 ns/Div; Vertical Scale, Positive Pulse Input: 5 V/Div; Output Settling: 1 mV/Div*

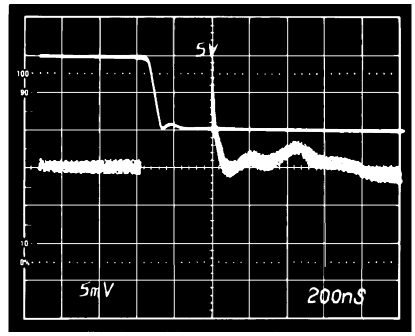



*Figure 28b. Settling Time of the Three Op Amp Instrumentation Amplifier. Horizontal Scale: 200 ns/Div; Vertical Scale, Negative Pulse Input: 5 V/ Div; Output Settling: 1 mV/Div*

**DRIVING THE ANALOG INPUT OF AN A/D CONVERTER**

An op amp driving the analog input of an A/D converter, such as that shown in Figure 29, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open-loop value. Most IC amplifiers exhibit a minimum open-loop output impedance of 25 Ω due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD845 is ideally suited to drive high resolution A/D converters with 5 µs on longer conversion times since it offers both wide bandwidth and high open-loop gain.

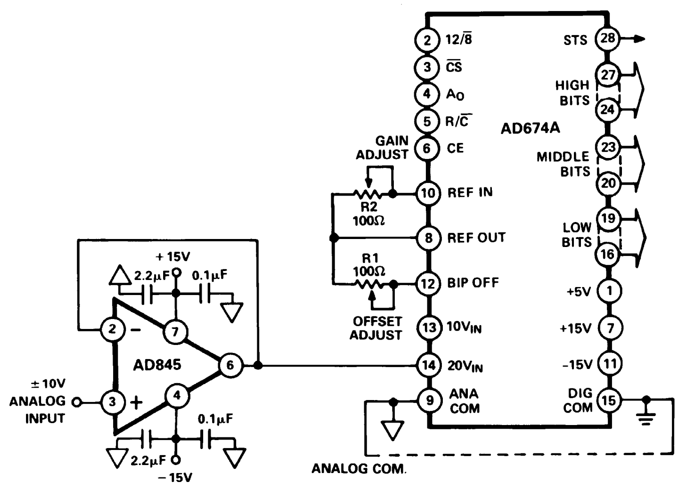
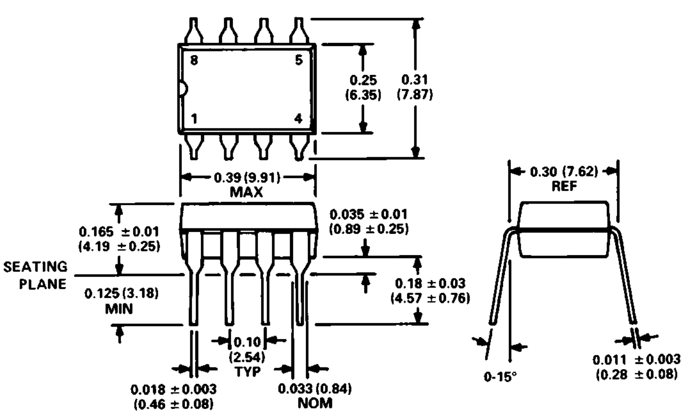



*Figure 29. AD845 As ADC Unity Gain Buffer*

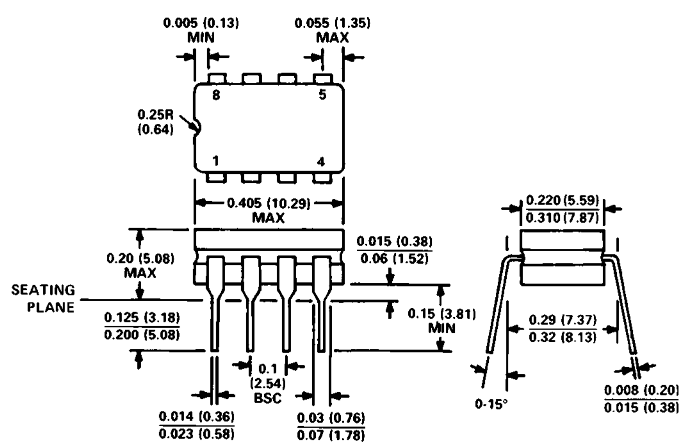
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**Mini-DIP (N) Package**




**Cerdip (Q) Package**




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